AMENDMENTS TO THE SPECIFICATION

Please replace paragraph beginning at page 4, line 12 with the amended paragraph/line as follows:

During a period for which the voltage VA is +VDD and voltage VB is 0, a current i will flow from the junction between FETs 151 and 152 to the junction between FETs 161 and 162 through a line extending from the low-pass filter 17 to the low-pass filter 18 via the speaker 19, as shown in FIGS. 1 and 3E. FIG 3F shows clock signal CLK.